CLAIMS:

What is claimed is:

1. A method of operating a processor comprising the steps of:

mapping at least a portion of a program memory space to a data memory space;

storing an entry into the program memory space that is mapped to the data memory space, the entry comprising data and a protection opcode;

fetching an entry from the program memory space;

attempting to execute the fetched entry;

trapping the protection opcode;

vectoring to a trap handler; and

executing the trap handler.

2. The method of claim 1, wherein the trap handler is an illegal instruction trap handler and the step of executing the trap handler comprises the steps of:

determining that the opcode is a protection opcode; and

executing a software routine to handle the trap.

3. The method of claim 2, wherein the program memory space is internal to the processor.

4. The method of claim 3, wherein the processor is operably connected to an external memory device operable to store program instructions and data, the external memory device comprising program memory space.

5. The method of claim 1, wherein the trap handler is a protection trap handler.

6. The method of claim 5, wherein the program memory space is internal to the processor.

7. The method of claim 6, wherein the processor is operably connected to an external memory device operable to store program instructions and data, the external memory device comprising program memory space.

8. A processor comprising circuitry operable to:

map at least a portion of a program memory space to a data memory space;

store an entry into the program memory space that is mapped to the data memory space, the entry comprising data and a protection opcode;

fetch an entry from the program memory space;

attempt to execute the fetched entry;

trap the protection opcode;

vector to a trap handler; and

execute the trap handler.

9. The processor of claim 8, wherein the trap handler is an illegal instruction trap handler and the execution of the trap handler comprises:

determining that the opcode is a protection opcode; and

executing a software routine to handle the trap.

10. The processor of claim 9, wherein the program memory space is internal to the processor.

11. The processor of claim 10, wherein the processor is operably connected to an external memory device operable to store program instructions and data, the external memory device comprising program memory space.

12. The processor of claim 8, wherein the trap handler is a protection trap handler.

13. The processor of claim 12, wherein the program memory space is internal to the processor.

14. The processor of claim 13, wherein the processor is operably connected to an external memory device operable to store program instructions and data, the external memory device comprising program memory space.